		continuously variable from 40 to 5000 times per second.
q.	Sweep delay and expansion	Allows any 10% of trace to be expanded by a factor of 9.
r.	Cathode ray tube:	
	Screen diameter	Three inches, 1½ inches total deflection, ¾ inch for pulse.
	CRT type	JAN 3WP1

SECTION 2
THEORY OF OPERATION

1. GENERAL ELECTRICAL CHARACTERISTICS OF OSCILLOSCOPE OS-57/USM-38 *(See figure 4-22, Block Diagram)*

a. VERTICAL DEFLECTION CHANNEL - The vertical deflection channel consists basically of a broad-banded amplifier having relatively flat frequency response from 10 cycles to 6 megacycles per second permitting the display of a large variety of waveshapes with little distortion. Sufficient attenuation and gain control is included in this amplifier to permit the application of signals in a wide range of magnitude. The circuit is arranged so that periodic, non-periodic, and random recurring waveshapes can be observed. When desired, the amplifier can be disconnected and connection made directly to the vertical deflection plates of the crt. The peak to peak voltage value of signals in the vertical channel can be measured by comparison with an internally generated

calibrated voltage. The signal for display is applied to the vertical channel at V INPUT jack J102. Attenuator AT101, V MULTIPLIER, is a six-position step attenuator controlling the input signal level to the Preamplifier circuits which include amplifier V101, and one-half V102 connected as a cathode follower to match the input impedance to Delay Line DL101. The calibrated comparison voltage, variable from 0 to 1 volt amplitude by the CAL VOLTS control is introduced to the vertical channel only when the CAL switch S102 is set in ON position. The second triode section of V102 is used to amplify a portion of the signal for use in synchronizing the sweep circuit. The delay line delays the signal in the vertical channel for approximately 0.4 microseconds; thus allowing the sweep to start slightly ahead of the vertical deflection. The Cathode Follower V103 circuit properly terminates the delay line and includes the continuously variable control V GAIN % R123. The signal is further amplified by the Vertical Driving Amplifier V104, to drive the push-pull Vertical Output amplifiers V105, V106. The vertical output is fed to the vertical deflection plates of the cathode ray tube V107. The input circuit to the vertical deflection plates includes the vertical positioning control V. POS and also the facilities for making direct connections.

b. HORIZONTAL DEFLECTION – The primary purpose of the internal sweep circuits is to develop a horizontal deflection voltage that varies linearly with time. Specialized circuits are included that control the sweep duration, repetition rate, and allow synchronization with signals from various sources.

(1) HORIZONTAL OUTPUT AMPLIFIER – This amplifier converts the positive going linear voltage output from the sweep circuits to a push-pull voltage which is applied to the horizontal deflection plates of the cathode ray tube. The sweep voltage input to this stage is clamped by V125B so that the horizontal deflection starts at the same point for all sweep waveforms and repetition rates. The horizontal positioning control H. POS is connected in the clamp circuit.

(2) GATE GENERATOR – This generator is a balanced multivibrator, using one-half of V121 and one-half of V122, and is

the timing circuit of the oscilloscope. It is either a repetitive or a driven multivibrator depending on the position of the SWEEP STABILITY control and the type of synchronization applied. It produces positive and negative gate pulses which actuate in synchronism the sweep, marker, and trace brightening circuits. The Gate Generator is coupled from the Sync Amplifier circuit through V121A, a diode connected triode, so that only positive going synchronizing pulses are effective at this point.

(3) SWEEP GENERATORS – The Sweep Generator consists of two parts; the Normal Sweep Generator and the Expanded Sweep Generator. The Normal Sweep Generator V124 is controlled by a negative going pulse from the Gate Generator. The width of the gate pulse, and thus the sweep duration, is controlled in steps by the SWEEP RANGE U SEC/IN control. Sweep speed is continuously variable for each step by the SWEEP SPEED control. The output of the Sweep Generator is coupled by the Sweep Amplifier (cathode follower) V123B via the H. GAIN control to either the Horizontal Output Amplifier or the Expanded Sweep Generator dependent on the position of S107 SWEEP EXP switch. In the OFF position of S107 the voltage output from the Sweep Amplifier V123B is applied directly to the Horizontal Output Amplifier. The Expanded Sweep Generator is active when S107 is moved away from its extreme counterclockwise "OFF" position. The expanded sweep generator is essentially an overdriven cathode coupled amplifier with a variable operating point (bias) so that any 10% portion of the normal sweep, selected by the SWEEP EXP control, is amplified. The starting point of the normal sweep input to the generator is held constant by the Expanded Sweep Clamp V125A.

c. SWEEP SYNCHRONIZATION – In order to synchronize the Gate Generator and thus the horizontal sweep voltage, a negative going sync signal must be applied to the Coupling Diode one-half V121 from the Sync Amplifier V120. Since the output polarity of V120 depends on its input polarity, the circuit of Sync Preamplifier V119 is arranged so that, regardless of the polarity of the sync signal input to the oscilloscope, a negative going output signal can be obtained. SYNC SELECTOR S104 is included to select the portion of the Sync Preamplifier required for negative going out-

put for either polarity sync signal applied. The SYNC SELECTOR S104 switch has five positions: +EXT, –EXT, +INT, –INT and TRIG. In the EXT positions the synchronizing signal must be supplied from an external source to EXT SYNC jack J109. In the INT positions the sync signal is obtained via the Int Sync Amplifier, one-half V102, from the vertical deflection channel. In the TRIG position a portion of the output pulse of the Trigger Generator V115 is picked off and used for a sync signal. The sensitivity of the Sync Amplifier V120 is varied by the SYNC SENS control R217.

d. TRIGGER GENERATOR – Trigger Generator V115 is a blocking oscillator active only when the SYNC SEL switch S104 is set in TRIG position. It supplies a positive pulse voltage, variable from 40 to 5000 cps by the TRIGGER RATE CPS control R182, via TRIGGER OUT jack J107 to external equipments requiring an actuating pulse. A fraction of the pulse output is applied internally (simultaneously) to the oscilloscope sweep synchronizing circuits.

e. INTENSITY (Z AXIS) CHANNEL – Control and modulation voltage applied to either the grid or cathode circuit of the cathode ray tube, affects the brightness of the screen presentation. The basic level of intensity is established by a dc bias which is varied by the INTENSITY control in the cathode circuit. The intensity is increased for the sweep duration through the introduction of the positive gate pulse to the control grid circuit of the crt. The gate pulse originating in the Gate Generator V121B and V122A is limited by the Intensity Gate Limiter V122B amplified by V123A, and shaped by Intensity Gate Shaper V108. When the MARKER U SEC switch S105 is set to Z AXIS position, brightening or blanking voltages originating in external equipment can be connected to the Intensity Channel at the panel jack J108, Z AXIS INPUT, through the marker Amplifier V118. When the MARKER U SEC switch is placed in 1, 10, or 100 position, time interval markers – appearing as bright dots evenly spaced on the trace – produced by the internal Marker Generator oscillator are amplified and shaped by the Marker Amplifier and fed to the cathode circuit of the crt. The Marker Generator is held in a non-oscillating condition by the Marker Gate V116 until unclamped by the negative gate pulse from the Gate Generator V121B, V122A, which also triggers the Sweep Gen-

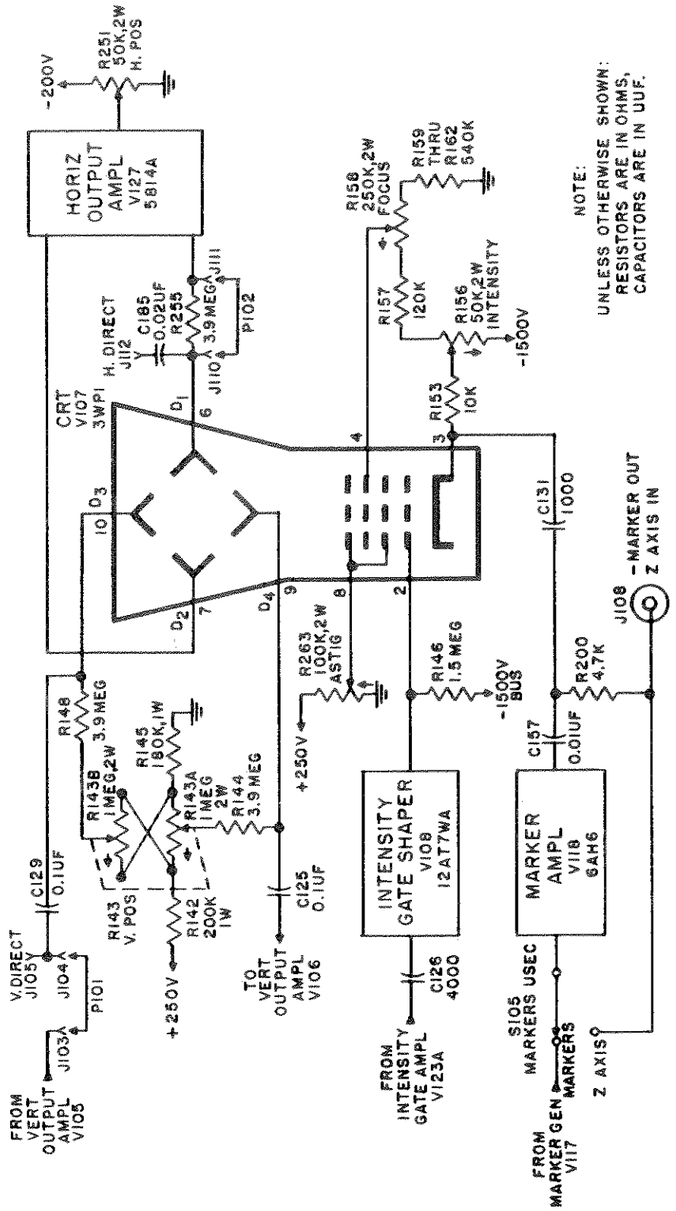

Figure 2-1. CRT Control Circuits, Simplified Schematic Diagram.

erator V124; thus insuring exact synchronism of the time interval markers with the sweep.

2. CIRCUIT ANALYSIS

a. VERTICAL DEFLECTION CHANNEL

(1) INPUT CIRCUIT AND V MULTIPLIER (See figure 2-2) – The signal from the circuit under test normally is applied at the V INPUT jack J102. A connection is made internally from pin A of the CF PROBE jack J101 to jack J102; thus applying the output of the cathode follower probe to the vertical channel. The Dummy Load DA-113/U when plugged into the CF PROBE jack presents a 75 ohm terminating impedance to the external circuit connected at V INPUT jack J102. Capacitor C102 prevents dc voltage from entering the V MULTIPLIER circuit. The V MULTIPLIER attenuator AT101 includes the six position rotary switch S101 which selects RC voltage dividing networks. Each network is arranged so that impedance presented to the circuit under test is constant and equal to 1 megohm shunted by 40 uuf. The attenuator is frequency and phase compensated so that minimum distortion of input signal results within the pass band of the vertical channel. When values of signal voltage input are compared with the internal calibrated voltage, the reading indicated by the CAL VOLTS control R154 must be multiplied by the setting of V MULTIPLIER attenuator. When the attenuator probe MX-1817/USM-38 is used an additional multiplier of 10 is required.

(2) VERTICAL PREAMPLIFIER AND DELAY CIRCUIT (See figure 2-4) – This circuit consists of (1) a resistance coupled pentode video amplifier, (2) a triode cathode follower V102A coupled to a delay line DL101, and (3) a triode connected pentode cathode follower V103 terminating the delay line. The gain through the Vertical Preamplifier V101 is approximately 4.5, and the gain through the cathode follower V102A, Delay Line DL101, cathode follower V103 combination is 0.42; therefore, the overall gain for this circuit is 1.9 as far as input signal to the Vertical Driving Amplifier V104 is concerned. Part of the vertical output of Cathode Follower V102A is coupled to the sweep synchronizing circuits via Internal Sync Amplifier V102B. In the following discussion the

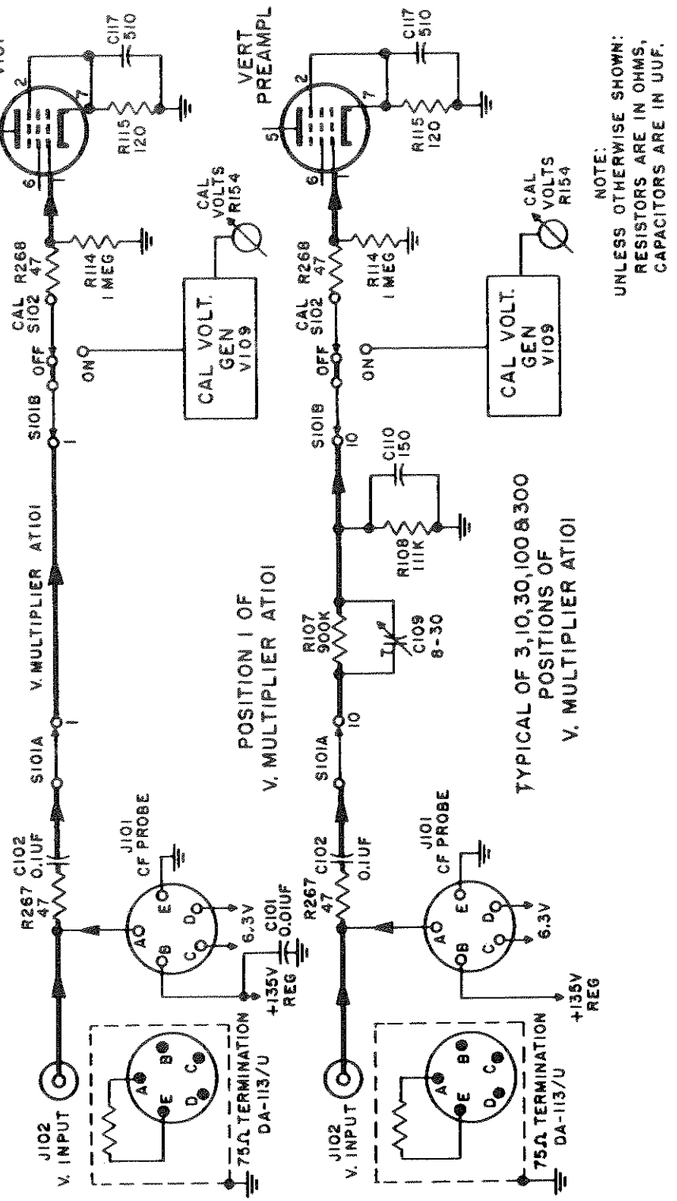

Figure 2-2. Input Circuit of V. Multiplier, Simplified Schematic Diagram.

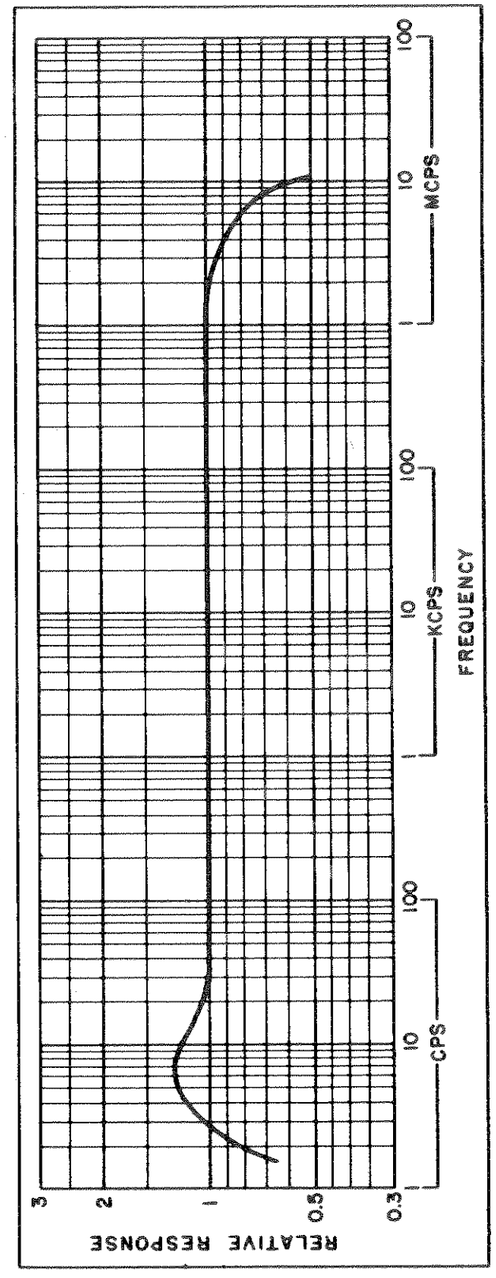

Figure 2-3. Frequency Characteristic of Vertical Channel.

CAL switch S102 is in the OFF position except when stated otherwise. The signal from the V MULTIPLIER attenuator is applied to the control grid of the Vertical Preamplifier V101. The output of the preamplifier is developed across the plate load resistors R112 and R113 and the coupling network C115, R116 and R117. Capacitor C116 across part of the plate load (R112) corrects phase distortion and also increases the response at low frequencies which tend to be attenuated by the capacitor C115 coupling the signal to the load resistors R116 and R117. To compensate for variations of circuit components from their nominal values, R117, CAL LOW FREQ is made adjustable; increasing the resistance increases the low frequency gain. The high frequency response is extended by bypassing the cathode resistor R115 for high frequencies with C117. Low shunt capacity of the input circuit of the next stage, a cathode-follower, also improves the high frequency response. In order to avoid serious attenuation, phase shift, and reflections, the delay line must be properly terminated at both ends in its characteristic impedance of approximately 1000 ohms resistive. This is accomplished by the coupling cathode-follower stages V102A and V103, respectively, at each end of the delay line. The cathode output impedance of V102A is increased to approximately 1000 ohms by the series resistor R119. The output end of the delay line is terminated directly in the matching 1000 ohm grid resistor, R122, input at V103. The output of V103, appearing across the cathode resistor R125 is coupled via capacitor C119 to the series combination of resistors R123 and R124, then from the arm of R123, V GAIN % to the grid of the Vert Driving Ampl V104. V GAIN % permits control of the gain of the vertical channel from 20% to 100% of the input level established by the attenuator V MULTIPLIER AT-101.

(3) VERTICAL DRIVING AMPLIFIER (See figure 2-5) – This stage consists of a frequency compensated RC coupled amplifier, using a pentode type 6AH6, V104, having a gain of approximately 4.5 sufficient to drive the succeeding output amplifier. The low frequency response of V104 is increased by using relatively large values for coupling capacitors C119 and C123 in the input grid, and output plate circuits respectively. The high frequency

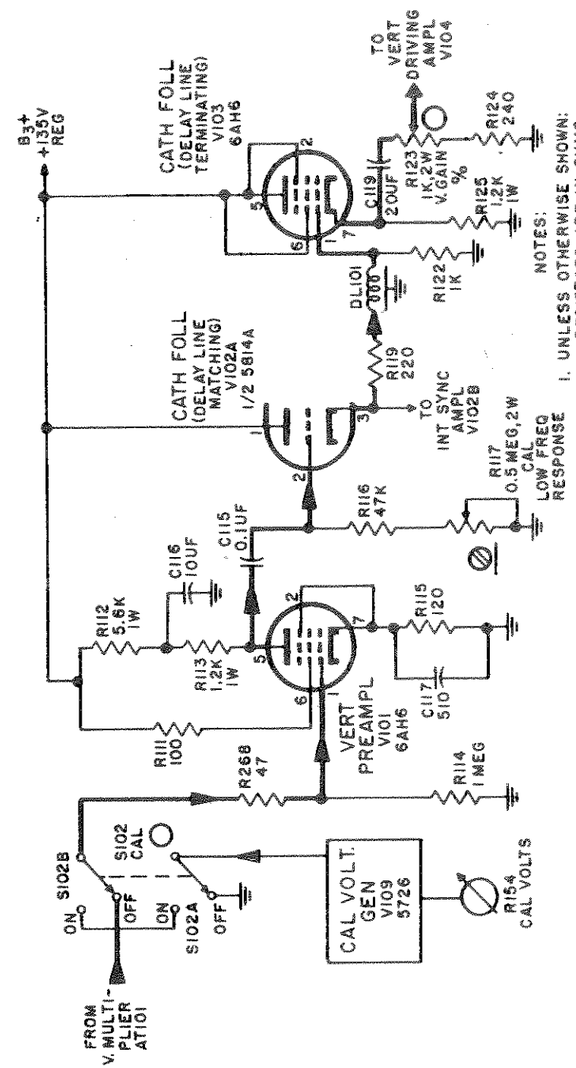

Figure 2-4. Vertical Preamplifier and Delay Circuit, Simplified Schematic Diagram.

response is extended by the shunt peaking coil L101 in the plate load, and through bypassing the cathode resistor R126 for high frequencies with capacitor C121. Screen operating voltage is furnished through the series dropping resistor R129. The network composed of R127 and C120 decouples the plate circuit of V104 from the power supply impedance and minimizes phase distortion. Capacitor C123 couples the output signal from the plate circuit of V104 to the input circuit of the Vertical Output Amplifier.

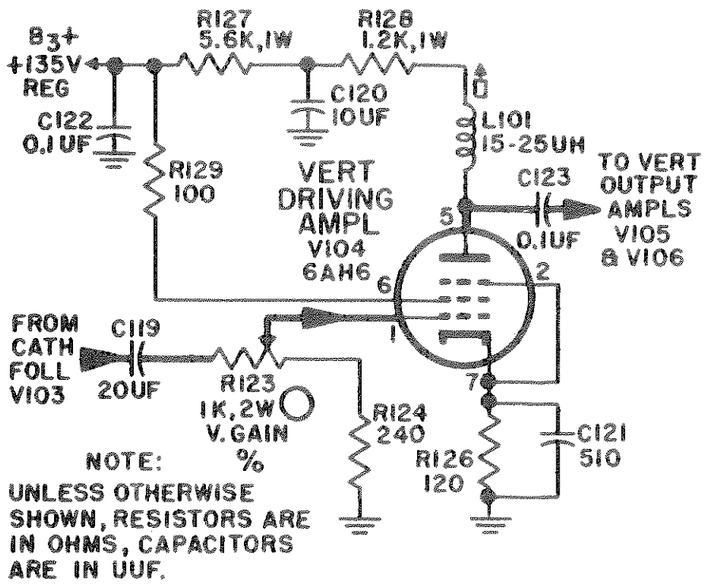

Figure 2-5. Vertical Driving Amplifier, Simplified Schematic Diagram.

(4) VERTICAL OUTPUT AMPLIFIER (See figure 2-6) – This stage includes two type 12BY7 pentodes V105, V106 connected in a cathode coupled amplifier circuit that converts the signal output from the single-ended Vertical Driving Amplifier, V104 to a push-pull signal output for the vertical deflection plates of the CRT, V107. The signal output from V104 coupled to the grid

of V105 causes a signal of following (same) polarity to appear across the unbypassed resistor R133 common to the cathodes of both V105, and V106. In effect, the voltage on the grid of V106 is then of opposite polarity, but of approximately equal amplitude. Actually, the grid of V106 is grounded, as far as the signal is concerned by means of bypass capacitor C124. The signals appearing in the balanced plate circuits of each tube thus are equal in amplitude but opposite in polarity, that is, push-pull. The low frequency response is extended by returning the grid resistors R132 and 134 to a common tap in the cathode resistance; thus increasing the effective grid resistance. High frequency response is extended by using both shunt and series peaking in the plate circuit to neutralize distributed capacitance. Screen voltage for the amplifiers is dropped through series resistors R138 and R137, R139. When the jumper plug P101 is removed, the amplified signal appears on one deflection plate and the V DIRECT signal on the other.

(5) CALIBRATING VOLTAGE GENERATOR (See figure 2-7) – This circuit includes a dual diode tube type 5726, V109, which is the source of a square-wave calibrating voltage used to determine, by substitution, the voltage amplitude of signals in the vertical channel. Complete instructions for making voltage measurements are given in paragraph 8 of Section 3 of this manual. The sine wave voltage of approximately 550 volts peak from terminal 5 of power transformer T101 is applied to V109 through limiting resistor R167. On the positive alternation the voltage is clipped at 150 volts because the pins 7, 1 diode of V109 has its cathode returned to +150 regulated supply and therefore conducts when its plate exceeds that value of bias. The negative alternation is removed entirely by the action of the pins 5, 2 of double-diode V109 which conducts directly to ground whenever its cathode becomes negative. The resulting 150 volts peak-to-peak, square-wave is applied to the series network of R166, R155 CAL SET, and R154 CAL VOLTS. R155 is a behind the panel adjustment used to set the voltage across the calibrated panel control R154, CAL VOLTS, to 1 volt peak-to-peak. The calibrated voltage is coupled from the arm of R154, via capacitor C113 to the CAL

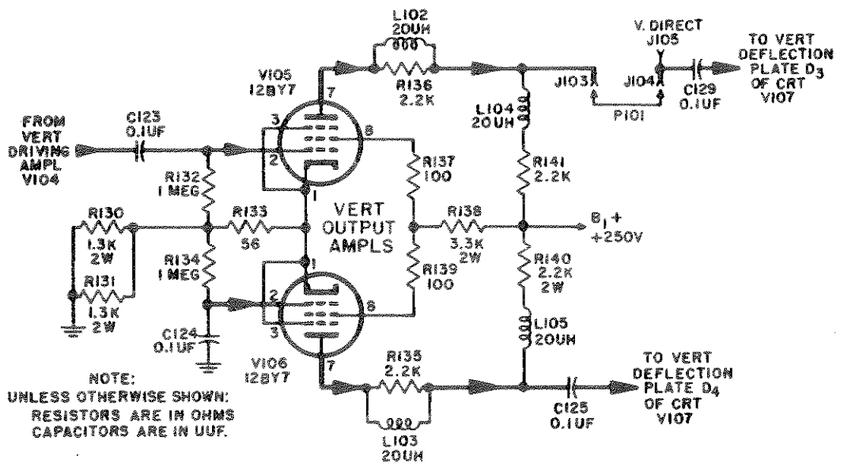

Figure 2-6. Vertical Output Amplifier, Simplified Schematic Diagram.

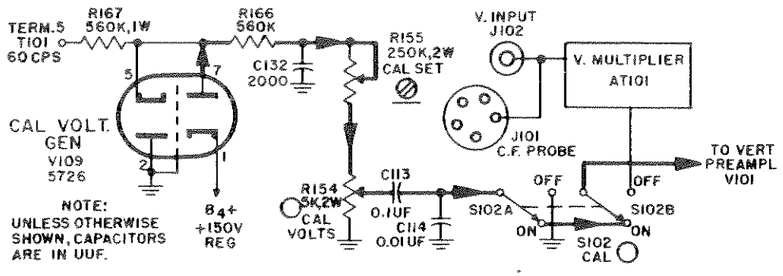

Figure 2-7. Calibrating Voltage Generator, Simplified Schematic Diagram.

switch S102. In the ON position, S102A connects the calibrated voltage to the grid of the Vertical Preamplifier V101; in the OFF position S102A disconnects the calibrated voltage and grounds it. Capacitor C114 bypasses to ground extreme high frequency components contained in the square wave.

(6) V. DIRECT CONNECTION (See figure 2-1) – Facilities for making direct connection to the vertical deflection plates are located beneath a gasketed plate on the back of the oscilloscope case (See figure 3-3). Before making connection to V. DIRECT jack J105, the jumper plug P101 must be pulled out in order to disconnect the vertical amplifiers. This permits direct connection to the vertical deflection plates with an impedance of 5 megohms shunted by approximately 30 uuf. Only unbalanced to ground (not push-pull), ac signals can be applied to J105. Vertical positioning is still available when direct connections are made since the positioning circuit including V POS control R143 is independent of the vertical amplifier. Negative going signals cause upward deflection of the beam.

(7) CRT CONTROL CIRCUITS (See figure 2-1). These circuits consist of the crt type 3WP1 and associated controls for static adjustments. The horizontal deflection plates are dc coupled to the Horizontal Amplifier V127. The H POS control R251 varies the bias on the grid of V127B, pin 2, changing the voltage of the push-pull output while substantially maintaining the average dc potential. The vertical deflection plates are ac coupled to the push-pull Vertical Output Amplifiers V105, V106. Vertical positioning is achieved by means of the cross connected dual potentiometers V. POS which produces a difference of potential between the deflection plates while maintaining their average dc potential. The ASTIGMATISM control R263 adjusts for optimum spot size throughout the deflection area. It compensates for electrical field unbalances, due to mechanical misalignment in the deflection plate structures, by adjusting the dc potential of the second anode, pin 8, with respect to the average dc potential of deflection plates D1, D2 and D3, D4. The FOCUS control R158 adjusts the dc voltage on the first anode resulting in a change of focus of the trace without affecting the beam current. The inten-

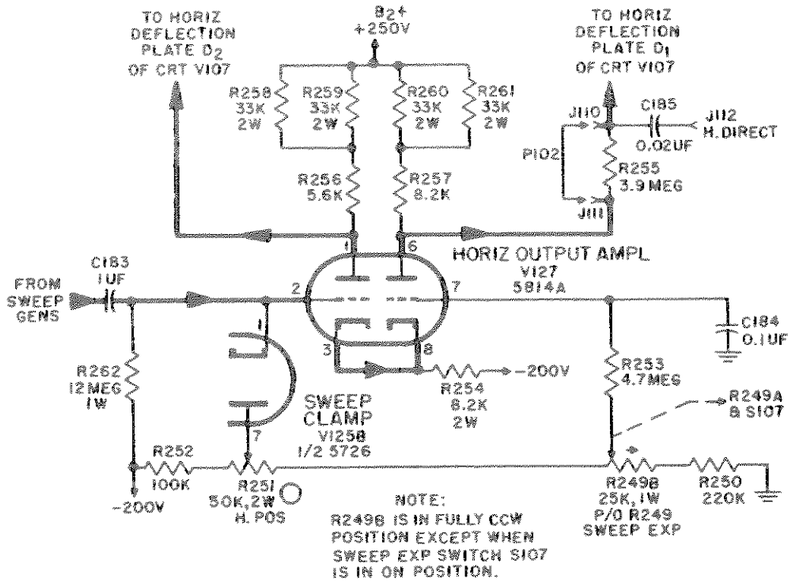

Figure 2-8. Horizontal Output Amplifier, Simplified Schematic Diagram.

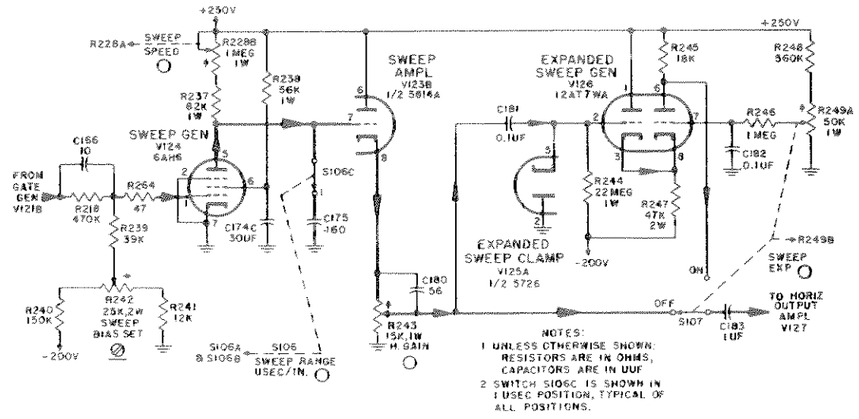

Figure 2-9. Sweep Generators, Simplified Schematic Diagram.

sity or brilliance of the trace appearing on the screen is adjusted by the INTENSITY control R156 which varies the cathode bias controlling the beam current of the tube.

b. HORIZONTAL DEFLECTION CHANNEL

(1) HORIZONTAL OUTPUT AMPLIFIER (See figure 2-8) – The Horizontal Output Amplifier, V127, consists basically of a dual triode type JAN5814A, connected in a cathode – coupled paraphase circuit which converts the unbalanced input voltage, from the sweep circuits, to balanced (push-pull) output for application to the horizontal deflection plates D1, D2 of the crt. Any voltage change on the grid of V127A causes a similar voltage to appear across the unbypassed cathode resistor R254 common to both V127A and B. With the grid grounded, the cathode voltage of V127B can be considered the same as its grid voltage but with opposite polarity. Thus the single-ended input signal causes plate signal outputs of V127A and B to be equal in amplitude but of opposite polarity, that is, push-pull. Coupling capacitor C183 and resistor R262 have a long time constant in order to pass the lower frequency sawtooth waveform with a minimum of distortion. The panel control R251, H. POS, controls the static bias on the grid of V127A, which varies the degree of voltage unbalance between the plates of V127, and changes the starting position of the sweep trace. The sweep signal input at the grid of V127A is clamped by the diode V125B, SWEEP CLAMP, to the value of negative bias set on R251. This dc restoration prevents horizontal jitter by insuring that each recurring trace starts from exactly the same position. Variable resistor R249B is effective only when the expanded sweep circuit is used. It serves to shift the whole trace slightly to the left as R249 SWEEP EXP is advanced, so that only the more useful section of the expanded sweep trace is presented on the screen. Capacitor C184 keeps the grid of V127B at signal ground potential. When direct connection is made to the H DIRECT jack J112 the jumper plug P102 must be removed from across resistor R255 which then isolates the deflection plate, D1, from the Horizontal Output Amplifier while still allowing positioning with the panel control H POS, R251.

(2) SWEEP GENERATORS (See figure 2-9) – The sweep circuits consist of the Sweep Generator V124, type JAN6AH6; Sweep Amplifier V123B, ½ type JAN5814A; and Expanded Sweep Generator V126, type JAN12AT7WA; which is not normally a part of the circuit; but is switched in only when the SWEEP EXP control R249 is advanced from its extreme counterclockwise "OFF" position. Sweep Generator V124 is normally conducting to a degree set by the behind-the-panel adjustment R242, SWEEP BIAS SET. Since V124 is heavily conducting, the charge on the sweep range capacitor selected by S106C is held at a low value. The output of the Gate Generator V121B, a negative-going rectangular wave, is direct-coupled to the grid of V124 via R218. The sweep is started when the leading edge of this negative gate quickly cuts off conduction in V124 thus allowing the sweep range capacitor (C175) to start charging toward the +250 supply voltage, at a rate governed mainly by the resistance of the SWEEP SPEED control R228B, for the duration of the gate. The trailing edge of the gate pulse restores V124 to its conducting condition and the sweep range capacitor in the circuit is rapidly discharged through the tube. This capacitor remains discharged until another gate pulse arrives at the grid of V124 at which time the sweep cycle repeats. Section R228B of the continuously variable SWEEP SPEED control and section S106C of the SWEEP RANGE switch, are separately ganged to R228A and S106 A and B respectively in the Gate Generator; these are so arranged that the duration of the gate is approximately one tenth of the time constant of the Sweep Generator circuit. This means that only the linear 10% portion beginning the exponential charging voltage on C175 is used for the sweep. Screen voltage is furnished V124 through the series dropping resistor R238. The screen is kept at ac ground potential at all times with bypass capacitor C174. The sweep voltage thus generated is direct coupled to Sweep Amplifier V123B, a cathode follower having a very low input capacitance, which isolates the Sweep Generator circuits from the loading effects of the succeeding circuits. In addition the cathode follower serves to match the low impedance of the H GAIN control R243; thereby reducing the effect of stray shunting capacitance in the control. Capacitor C180 provides high frequency compensation to prevent the sawtooth waveforms from rounding off at the beginning and ending of the

slope. During normal operation the sweep voltage is coupled via S107 and C183 to the Horizontal Output Amplifier V127. The expanded Sweep Generator V126 is effective only when the SWEEP EXP panel-control R249 is turned from its extreme counterclockwise position actuating S107 which then switches the input circuits of the Horizontal Amplifier, V127, to the output circuit of V126B. The normal sawtooth wave forms from the Sweep Amplifier V123B is ac coupled to V126A, a cathode follower, via C181 and R244 which have the long time constant required to pass the lower frequency components of the wave. Since the Sweep Ampl is ac coupled to the sweep expansion circuit, the diode section V125A is used to clamp the beginning of the sawtooth waveform to ground potential. V126A is cathode coupled (by the common cathode resistor R247) to the amplifier V126B; therefore the bias on V126A is controlled by the SWEEP EXP control R249A. When SWEEP EXP control is fully counterclockwise a small bias voltage is present on the cathode follower V126A, and the entire sawtooth voltage is cathode coupled to the limiter V126B. However, as R249A is advanced the bias on V126A increases gradually to cutoff and beyond, until at full clockwise rotation, only the top portion of the sawtooth is coupled to V126B. V126B amplifies by approximately 9 times and then limits the positive swing to prevent overloading of the Horizontal Output Amplifier. The result is that any 10% of the normal sweep can be expanded and sufficiently delayed to become visible on the screen. The expanded sweep voltage is developed across the plate load resistor R245 and is coupled via capacitor C183 and S107 to the push-pull Horizontal Output Amplifier V127.

(3) GATE GENERATOR (See figure 2-10) – The Gate Generator is basically a flip-flop type multivibrator using two triodes, V121B one-half JAN12AT7WA, and V122A one-half JAN5814A. In normal operation the Gate Generator is driven, each cycle, by a triggering voltage from the Sync Amplifier V120 through Coupling Diode V121A, one-half JAN12AT7WA. A free-running condition can be obtained at a point on the SWEEP STABILITY control, R220, with clockwise rotation. In the driven condition, V121B is the normally-off tube and V122A the normally-on (i.e. conducting). Coup-

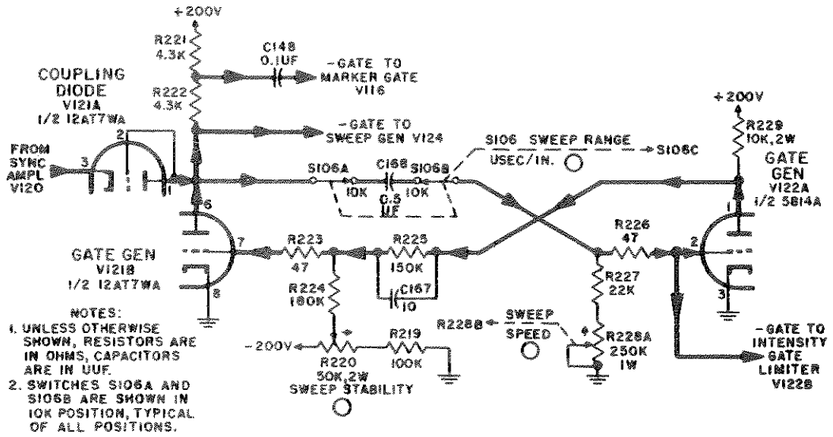

Figure 2-10. Gate Generator, Simplified Schematic Diagram.

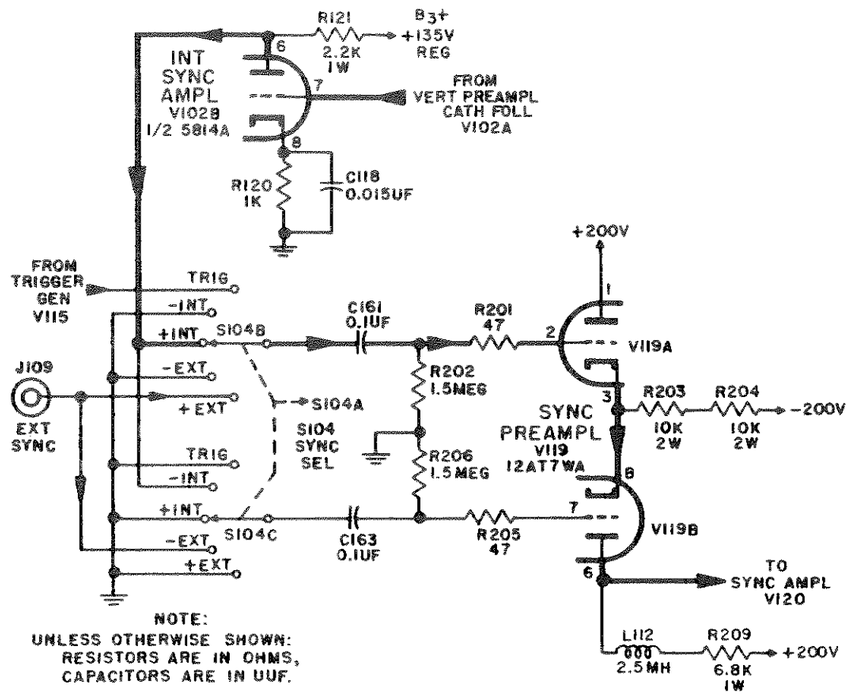

Figure 2-11. Sync Selector Switch and Sync Preamplifiers, Simplified Schematic Diagram.

ling Diode V121A can pass only the negative-going portion of sync signals from V120. In normal operation, the leading edge of the sync signal, coupled via C168 to the grid of V122A, tends to cut off conduction in that tube and produces at the plate (pin 1) an amplified positive-going signal which, via R225, drives V121B into conduction so that its plate (pin 6) becomes more negative. This regenerative action cuts off V122A and saturates V121B almost instantly. After a period of time determined by the value of capacitance (C168 in Fig. 2-10) selected by the SWEEP RANGE U SEC/IN switch S106, and the value of resistance set on R228A, SWEEP SPEED, the circuit flops back into its stable condition. This action results in equal negative-going output rectangular waves at R221 and R222 in the plate circuit of V121B, which are used to gate the Marker Generator and the Sweep Generator respectively. A negative-going peaked wave signal produced at the grid (pin 2) of V122A is applied to the Intensity Gate forming circuits. Because the time of occurrence and the time-base of these three gate voltage sources is necessarily the same, the result is exact synchronism of the three gated circuits. As the SWEEP STABILITY control R220 is advanced clockwise, a bias point is reached where V121B becomes conducting; the oscillation described above will start and continue repetitively, with or without a sync signal.

(4) SYNC CIRCUIT (See figure 2-11) – The Sync Circuit consists basically of Sync Preamplifier V119, type JAN12AT7WA, Sync Amplifier V120, type JAN5814A, and the SYNC SEL switch S104. The circuit is so designed that the Gate Generator can be synchronized to either the positive or the negative going portion of a sync signal originating either internally or in external equipment. In normal operation, the leading edge of the sync signal is used to trigger the sweep circuit so that the whole of the signal in the Vertical Channel will be displayed. SYNC SEL switch S104 adapts the sync circuits to both the polarity and the source of the sync signal. In +EXT position the positive going portion of a signal originating in equipment external to the oscilloscope is used for sync purposes. Jack J109 EXT SYNC is connected via S104B and the coupling capacitor C161 to the grid of the cathode follower section V119A. S104C now connects directly to ground the grid capacitor

C163 of V119B. V119A passes the sync signal without polarity inversion. V119B, now connected as a grounded-grid amplifier coupled by cathode resistor R203, also passes the signal without inversion via C162 to V120A (See figure 2-12). V102A is a cathode-follower with its output developed across R210, again uninverted, coupled by C164 to the conventional amplifier V120B which does invert the polarity of the signal so that only the portion that started with positive-going polarity will pass the Coupling Diode V121A (which passes only negative-going signals) and synchronize the Gate Generator, which in turn triggers the Sweep Generator. The gain of the Sync Amplifier is controlled by the SYNC SENS control R217 which varies the grid bias for V120B. In –EXT position the negative going portion of the external sync signal is used. Jack J109 is switched via S104C and coupling capacitor C163 to the grid of V119B. S104B switches the cathode-follower V119A out of the circuit by grounding its input grid circuit at C161. V119B, now connected as a conventional amplifier, inverts the sync signal to the necessary positive-going polarity required before it is couped via capacitor C162 to the Sync Amplifier V120 which functions as described above. In the +INT position of S104, the positive going portion of the undelayed signal in the Vertical Channel is used for sync purposes. The output of the conventional Int Sync Amp V102B is switched by S104B to the input of the cathode follower V119A. The grid circuit of V119B is grounded by S104C. With the exception of the source of the signal, the Sync Circuit then functions as described under +EXT above. In the –INT position of SYNC SEL switch S104, the negative-going portion of the vertical signal is used for sync purposes. The output of Int Sync Amp V102B is switched by S104C to the grid of V119B connected as a conventional amplifier. S104B disables the cathode follower V119A. The Sync Circuit, with the exception of the signal source, then functions as described under –EXT position above. In TRIG position, S104 picks off a fraction of the positive-going output pulse from V115, Trigger Gen, for use as synchronizing voltage. S104B introduces the signal into the grid circuit of the cathode follower V119A. S104C connects V119B as a grounded grid amplifier. From

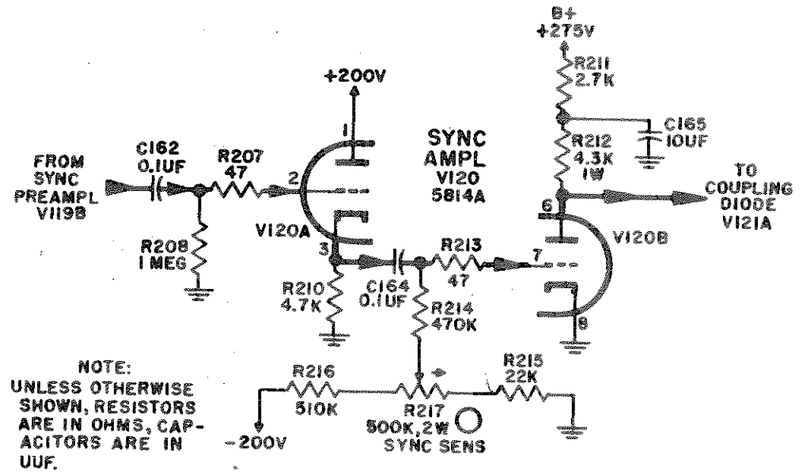

Figure 2-12. Sync Amplifiers, Simplified Schematic Diagram.

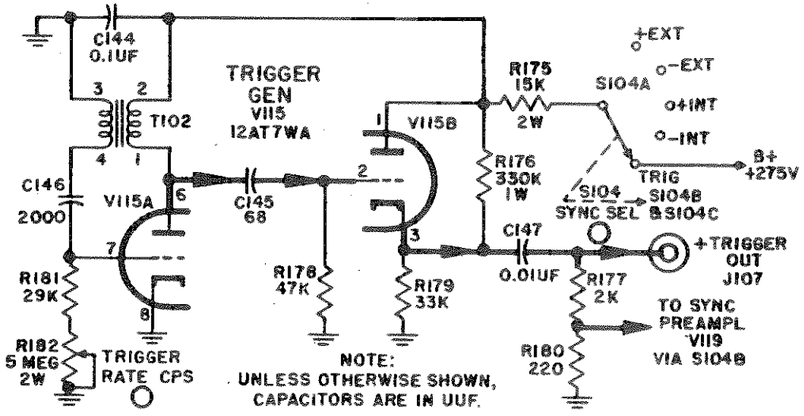

Figure 2-13. Trigger Generator, Simplified Schematic Diagram.

this point on, the sync circuit then functions for positive-going signals as described under +EXT above.

(5) TRIGGER GENERATOR (See figure 2-13) – This circuit uses a dual-triode type JAN12AT7WA, V115. It becomes active only when plate voltage is connected by placing the SYNC SEL switch S104 in TRIG position; at which time, sharp positive going output pulses of approximately 100 volts peak, having a rise time of 0.5 microseconds, continuously variable in frequency from 40 to 5000 cps by the panel-control TRIGGER RATE CPS, are available at jack J107 + TRIGGER OUT for the triggering of external equipment. A portion of output trigger pulse is introduced via SYNC SEL switch S104 to V119, Sync Preamp, in order to initiate the sweep circuits in proper synchronism. V115A is a triode blocking oscillator. Plate to grid feed-back through pulse transformer T102 drives the grid positive during half the cycle. Sufficient grid current flows into C146 during a small fraction of the half cycle to block further oscillation until the charge on the grid leaks off through R181 and the TRIGGER RATE CPS control R182. Thus the output of V115A is a series of sharp pulses whose repetition rate is governed by the setting of R182. Because of overshoot in T102 both positive and negative going pulses appear at the plate of V115A. These pulses are coupled via C145 to the grid of V115B which is biased sufficiently negative that only positive peaks are passed. These pulses appear across the cathode resistor R179 and are coupled by C147 to +TRIGGER OUT jack J107. Pulses for application to the Sync Preamp V119 are picked off at the junction of dividing resistors R177 and R180.

c. INTENSITY (Z AXIS) CHANNEL (See figure 2-14 and 2-15)

(1) INTENSITY GATE CIRCUITS – The intensity gate circuits increase the brightness of the crt display only during the forward trace of the sweep. The increase in intensity is necessary to maintain constant brightness level during sweep time and also to eliminate the return trace. The circuit includes Intensity Gate Limiter V122B, one-half 5814A and crystal diode CR101, Intensity Gate Amplifier V123A, one-half 5814A, and Intensity Gate Shaper V108, 12AT7WA. V122B is normally conducting and maintains a voltage drop across its plate load resistor R232 large enough to

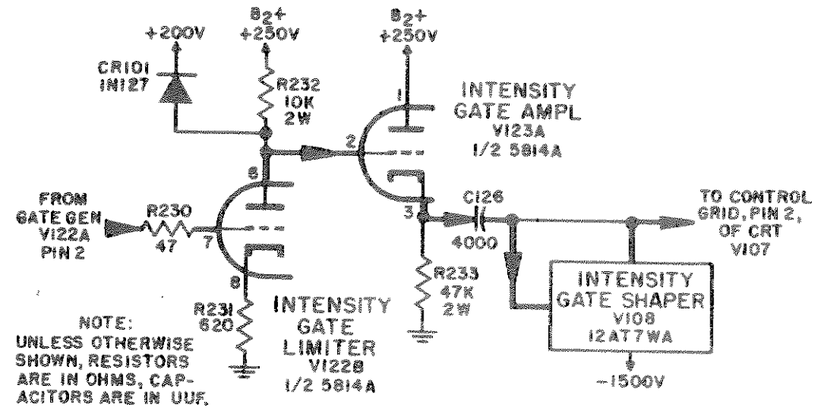

Figure 2-14. Intensity Gate Amplifier, Simplified Schematic Diagram.

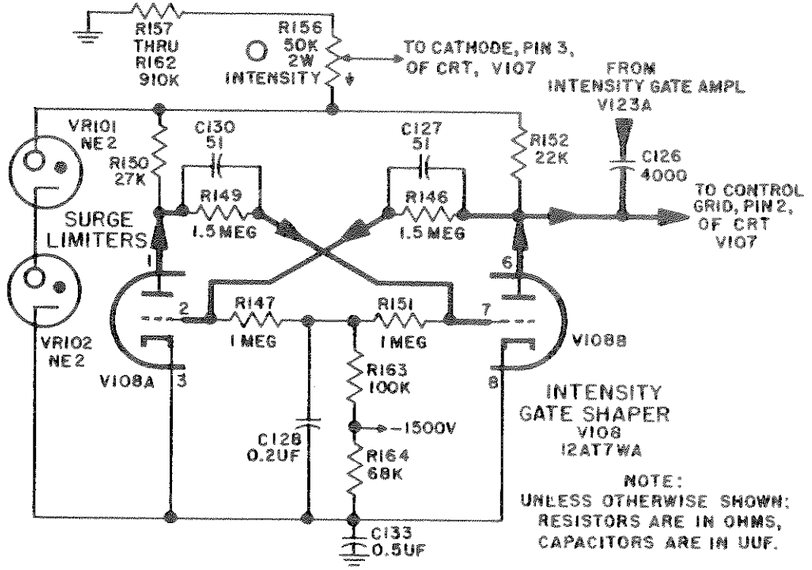

Figure 2-15. Intensity Gate Shaper, Simplified Schematic Diagram.

prevent the diode CR101 from conducting. The diode is returned to plus 200 volts supply while the plate load is returned to plus 250 volts supply. The negative going gate pulse, originating in the Gate Generator V122A tends to cut-off V122B, causing the plate voltage to rise toward 250 volts; however, it can rise no higher than 200 volts since at this point the diode CR101 begins to conduct; thus limiting the amplitude and flattening the top of the positive going gate pulse. The output of V122B is direct-coupled to the grid of V123A, a cathode follower, and the output developed across the cathode resistor R233 is coupled, via capacitor C126, simultaneously to the grids of the crt V107, and the Intensity Gate Shaper V108. V108 is a bi-stable multivibrator used to improve the shape, at low frequencies, of the intensity gate applied to the grid of the crt. At high frequencies the intensity gate is sufficiently well shaped to turn the beam on at the beginning of the sweep. In the latter case, the gate passes from C203 directly to the grid of the cathode ray tube. At lower frequencies the rising edge of the intensity gate is applied simultaneously to the grid of V108A, normally at cutoff, and to the plate of V108B, normally conducting, causing the multivibrator to switch rapidly to its second stable condition, that is, V108A conducting and V108B at cutoff. This action causes the square wave output of V108B to be superimposed on the intensity gate. V108 remains in the second condition until the falling edge of the intensity gate signal causes a rapid switch back to the normal condition. Operating voltages for V108 are obtained by tapping across part of the negative high voltage divider. To prevent the full negative high voltage surge from being impressed upon the circuit when the oscilloscope is first turned on, the neon bulbs VR101 and VR102 fire and maintain a safe value of voltage until the tubes heat up and the circuits stabilize; then the neon bulbs stop glowing and are no longer part of the circuit.

(2) MARKER GENERATOR (See figure 2-16) – The Marker Generator is basically a gated multivibrator whose output is used to supply markers of known time intervals to the Z Axis of the crt. The basic circuit uses V116, Marker Gate, type JAN6AH6; and V117, Marker Generator, a dual-triode type JAN12AT7WA. This cir-

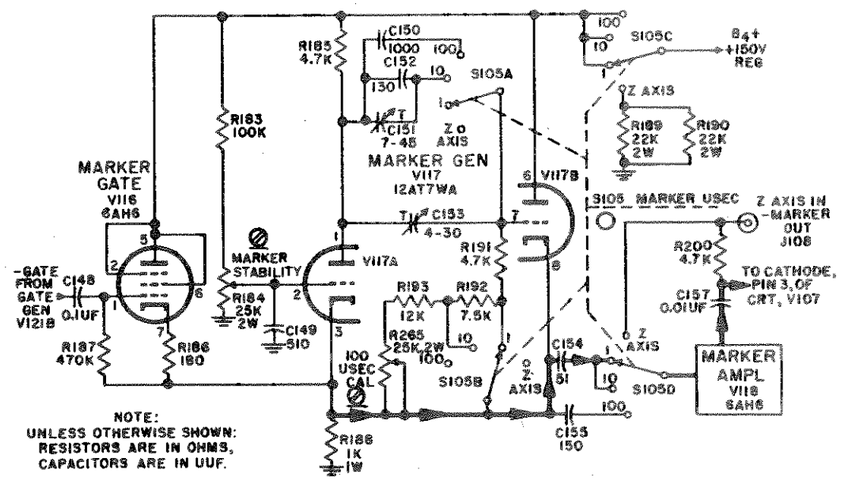

Figure 2-16. Marker Generator, Simplified Schematic Diagram.

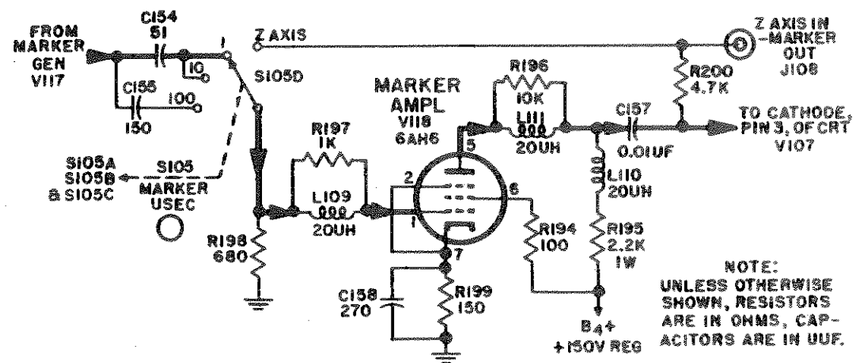

Figure 2-17. Marker Amplifier, Simplified Schematic Diagram.

cuit is activated only when the MARKERS U SEC switch S105 is placed in one of the 1, 10, or 100 positions. The two triodes V117A and V117B are coupled by the common cathode resistance R188. The multivibrator action is normally held quiescent with the large bias voltage developed across cathode resistor R188 due to the high current drawn through it by the Marker Gate tube V116. Upon the arrival of a negative-going gate signal (from Gate Generator V121B) at its grid, V116 is rapidly cutoff; thus removing the additional bias from V117A and B which then begin to oscillate at a rate determined by the values of capacitance and resistance selected by switch sections S105A and S105B respectively. The behind-the-panel control MARKER STABILITY, R184, adjusts the sensitivity of V117A. The output pulses of the Marker Generator are coupled via either C154 or C155 (the smaller value of C154 is used to insure passage of the highest frequency components of the 1 and 10 microsecond interval markers) to the Z Axis Amplifier V118 where they are peaked, amplified, and coupled to the cathode of the crt. The trailing edge of the negative gate pulse returns V116 to its conducting condition cutting off the Marker Generator V117 which remains quiescent until again gated. When the MARKER U SEC switch S105 is in the Z Axis position the Marker Generator is disabled by removing the plate voltage, pin 6, for V117B. The gating of the Marker Generator insures exact synchronism of the markers with the Sweep and Intensity circuits.

(3) MARKER AMPLIFIER AND Z AXIS INPUT (See figure 2-17) – The Marker Amplifier V118 is basically a conventional single-ended audio amplifier using a type JAN6AH6. It functions to amplify either the timing markers from the internal Marker Generator V117 or external signals connected at Z AXIS IN jack J108 depending on position of the MARKER U SEC switch S105. In either case the high frequency response is compensated for by series peaking in the grid circuit (L109), and with series and shunt peaking in the plate circuit (L111 and L110 respectively). The small value of the cathode bypass capacitor C158 also increases the high frequency response. In any of the 1, 10, or 100 positions of S105 the grid circuit of V118 is connected to the output of the Marker Generator V117 via either coupling capacitor C154 or C155 and

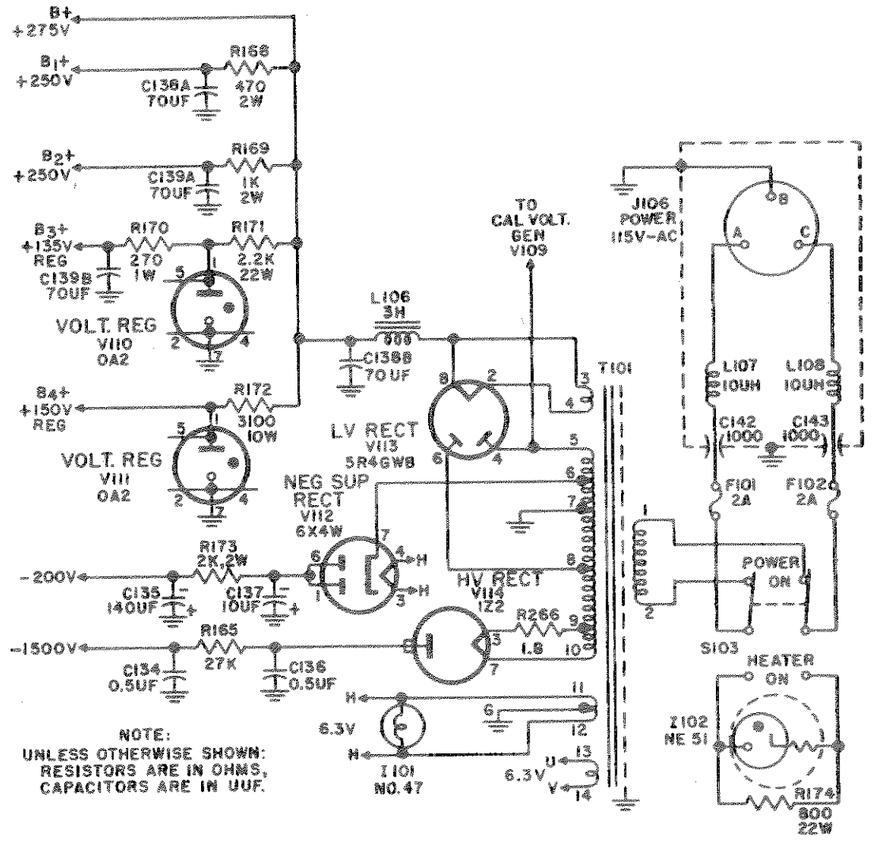

Figure 2-18. Power Supply, Simplified Schematic Diagram, See Note 6, Table 5-3.

the grid resistor R198. The short time constant of this RC combination sharply peaks the marker pulses. The amplified output marker signals are applied to the cathode circuit of the crt through capacitor C157. The marker output is also connected, through R200, to –MARKER OUT jack, J108, with an internal impedance of 5.7K ohms and 3 volts peak open circuit. In the Z AXIS position, S105 disables the Marker Generator V117 and also connects J108, in its Z AXIS function, directly to R198 in the grid circuit of V118. The amplified external signal is coupled to the cathode circuit of the crt via C157, R200 isolates J108 from the output plate circuit. In Z AXIS IN function the input impedance at J108 is 680 ohms.

SECTION 3
INSTALLATION AND OPERATION

1. UNPACKING

a. Oscilloscope Set AN/USM-38 and a set of equipment spares are packed in a V3c board carton. Electron tubes are shipped in place. Within the carton Oscilloscope AN/USM-38 (with its accessories stored inside its cover) and the set of spares are packed in individual cardboard containers.

b. Use care when opening the containers in order to avoid damaging their contents.

2. INSTALLATION

Because Oscilloscope AN/USM-38 is a portable equipment, no

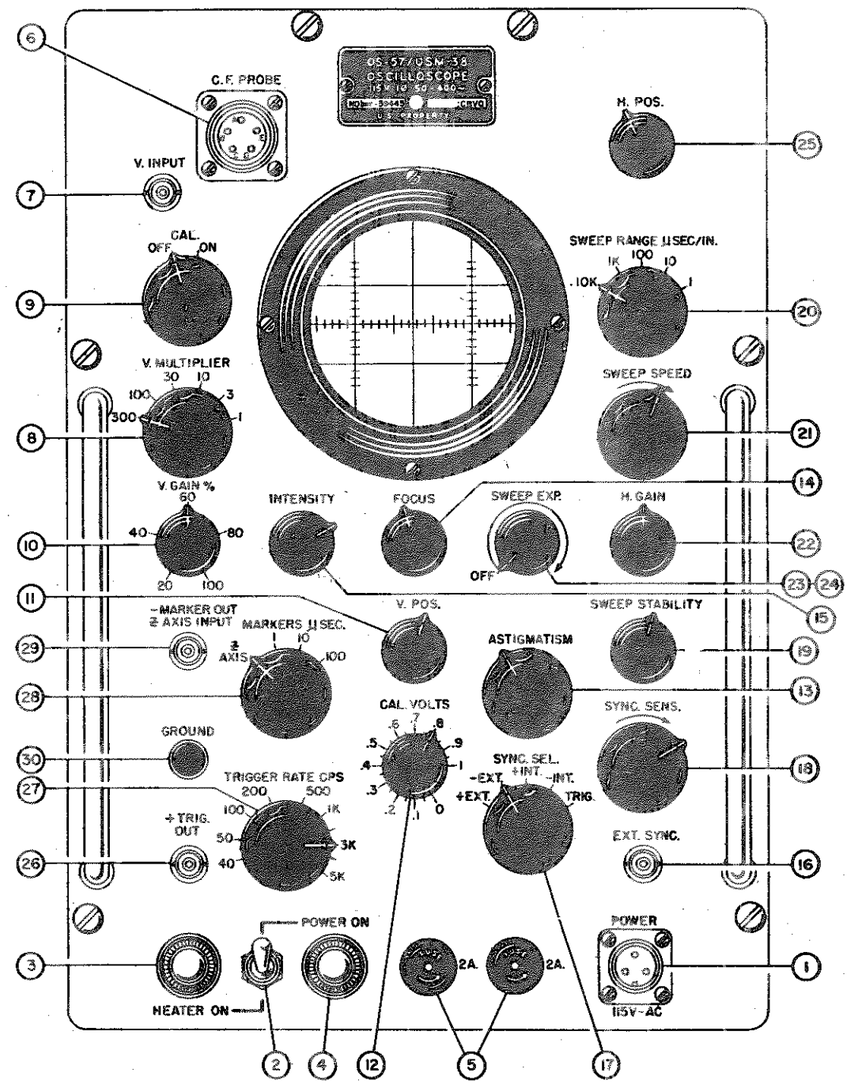

Figure 3-1. Operating Controls and Connectors, Oscilloscope OS-57/USM-38.